Single-Chip Multi-Port Ethernet Switch

ABSTRACT

An architecture for a multi-port switching device is described having a very regular structure that lends itself to scaling for performance speed and a high level of integration. The distribution of packet data internal to the chip is described as using a cell-based TDM packet transport configuration such as a ring. Similarly, a method of memory allocation in a transmit buffer of each port allows for reassembly of the cells of a packet for storage in a contiguous manner in a queue. Each port includes multiple queues. The destination queue and port for a packet is identified in a multi-bit destination map that is prepended to the start cell of the packet and used by a port to identify packets destined for it. The architecture is useful for a single-chip multi-port Ethernet switch where each of the ports is capable of 10 Gbps data rates.